ABSTRACT

Various embodiments of the invention relate to communicating data between a number of processing elements (PEs) of a signal processor, using a plurality of communication registers (CCRs). For instance, a plurality of the CCRs can be shared by and mapped to the address space of each PE, where each CCR couples a first of the PEs to every other one of the PEs. Moreover, each CCR can include a data payload field and a data valid field to indicate a target PE to read the data in the data payload field. Thus, data can be written to a selected CCR by a PE and stored in the selected CCR to be read by at least one target PE.